PATENT ABSTRACTS OF JAPAN

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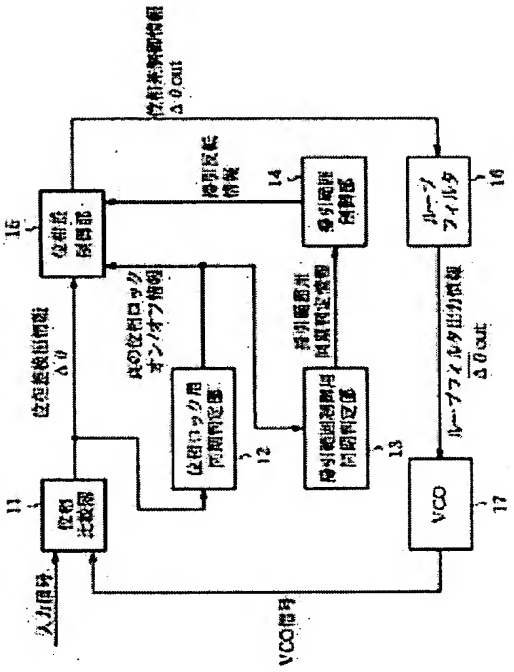
(54) PHASE SYNCHRONIZATION LOOP CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To solve the problem that it takes a long time for locking the true frequency and for bringing over because sweeping control in the entire range is carried out and even unnecessary frequency is swept even thought he frequency is not considerably deviated soon after a true phase lock off has occurred.
SOLUTION: After a true phase lock off has been judged, first phase difference detecting information having a narrow range of sweeping frequency is outputted until a predetermined time passes away. After the lapse of the predetermined time, second phase difference information having a broader range of sweeping frequency than that of the first phase difference detecting information is outputted.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]When this invention will be in an asynchronous state, it relates to the phase synchronous loop circuit drawn in a synchronous state using the phase difference detecting information for a sweep.
[0002]
[Description of the Prior Art]A phase synchronous loop circuit is also called PLL (Phase Locked Loop), and performs closed-loop processing which comprises a phase comparator, a loop filter, and VCO. Generally, in a phase-locked loop, when the frequency of an input signal and a VCO signal differs extremely, special processing called the sweep processing using open loop processing may be performed.
[0003]In [drawing 6 is a lineblock diagram showing the conventional phase synchronous loop circuit shown in JP,2-100348,A, and] a figure, The phase comparator which 1 compares the phase of an input signal and a VCO signal, and outputs the comparison result as phase-difference-detecting-information deltatheta, The synchronization judging part for phase locks which judges a synchronous state based on phase-difference-detecting-information deltatheta to which 2 was outputted from the phase comparator 1, 3 is a sweep range control section which outputs sweep reversal information (phase contrast control information for a sweep), when a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.
[0004]When 4 is judged by the synchronization judging part 2 for phase locks to be the phase lock on of truth [synchronous state], It outputs to the loop filter 5 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 1, The phase contrast control section outputted to the loop filter 5 by making into the phase contrast control information deltathetaout the sweep inversion signal outputted from the sweep range control section 3 when a synchronous state is judged to be true phase lock OFF, The loop filter which smooths the phase contrast control information deltathetaout to which 5 was outputted from

the phase contrast control section 4, and 6 are VCO which outputs as a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 5.

[0005]Next, operation is explained. Operation of the closed-loop processing in a phase synchronous loop circuit is explained to the beginning. First, the phase comparator 1 compares the phase of an input signal and a VCO signal, sets the comparison result to phase-difference-detecting-information deltatheta, and outputs to the synchronization judging part 2 for phase locks, and the phase contrast control section 4.

[0006]The synchronization judging part 2 for phase locks will judge a synchronous state based on the phase-difference-detecting-information deltatheta, if phase-difference-detecting-information deltatheta is received from the phase comparator 1. That is, it is judged whether the present synchronous state is true phase lock on or it is true phase lock OFF. A phase synchronous loop circuit performs closed-loop processing, when the present synchronous state is true phase lock on, when it is true phase lock OFF, perform open loop processing, but. When judged with the decision processing in the synchronization judging part 2 for phase locks having [more than the number of times of regulation] phase-difference-detecting-information deltatheta smaller than the value judged to be phase lock on, it is judged with a true phase lock on state. Conversely, when more than the number of times of regulation judges that phase-difference-detecting-information deltatheta is larger than the value judged to be phase lock OFF, it is judged with a true phase lock OFF state.

[0007]The phase contrast control section 4 will be outputted to the loop filter 5 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 1, if a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock on. This processing is continued until a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.

[0008]The loop filter 5 will perform data smoothing of the phase contrast control information deltathetaout, if the phase contrast control information deltathetaout is received from the phase contrast control section 4. VCO6 is outputted to the phase comparator 1 by making into a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 5. If repeat execution of each processing in phase comparator 1, phase contrast control-section 4, loop filter 5, and VCO6 is carried out, the phase contrast of an input signal and a VCO signal will decrease gradually, and will become almost the same [the phase of an input signal and a VCO signal], and a phase lock will be materialized.

[0009]Next, operation of the open loop processing in a phase synchronous loop circuit is explained. Since the processing in phase comparator 1, synchronization judging part 2 for phase locks, loop filter 5, and VCO6 is the same as that of the case of closed-loop processing, explanation is omitted. The sweep range control section 3 will output sweep reversal information (phase contrast control information for a sweep) to the phase contrast

control section 4, if a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.

[0010]The sweep range control section 3 outputs sweep reversal information to the phase contrast control section 4 so that the phase contrast of the output signal of the loop filter 5 may repeat with increase [in increase -> reduction ->] ->--. This processing is mainly performed using a counter, the time of the decision result of the synchronization judging part 2 for phase locks becoming true phase lock OFF is made into a trigger, and whenever it counts only regulation counted value, the polarity of sweep reversal information is reversed.

[0011]If a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF, the phase contrast control section 4, It outputs to the loop filter 5 by making into the phase contrast control information deltathetaout the sweep reversal information outputted from the sweep range control section 3, without outputting phase-difference-detecting-information deltatheta outputted from the phase comparator 1. This processing is continued until a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock on.

[0012]Although operation of the loop filter 5 is the same as that of the time of closed-loop processing, the smoothed phase contrast which is an output signal of the loop filter 5 increases [fixed-] or decreases [fixed-] it under the influence of the integrator in the loop filter 5 by the ability to give fixed phase contrast. Since phase contrast is considered to be the differentiation of a phase value, i.e., frequency, that phase contrast increases means that frequency increases. That phase contrast decreases similarly means that frequency decreases.

[0013]Therefore, the frequency of the VCO signal outputted from VCO6 becomes possible [creating the state where it becomes the operation which continues sweeping the normal frequency range, and the frequency and the phase of the input signal and VCO signal of a phase synchronous loop circuit become the same] by inputting fixed phase contrast into the loop filter 5. The frequency of a VCO signal needs to sweep the regulation sweep range of this frequency in the range which can respond even when the frequency of the input signal of a phase synchronous loop circuit shifts.

[0014]

[Problem(s) to be Solved by the Invention]Since the conventional phase synchronous loop circuit is constituted as mentioned above, after the phase lock on of once truth is materialized, when judged with true phase lock OFF by the influence of noise etc., change into an open loop state from closed-loop processing, and perform the frequency sweep of VCO6, but. In order to carry out sweep control of a total range and to sweep to excessive frequency in spite of not shifting frequency greatly when true phase lock OFF has just arisen, the long time was taken to lock true frequency and SUBJECT that level luffing motion took time occurred.

[0015]It was made in order that this invention might solve above SUBJECT, and it aims at

obtaining the phase synchronous loop circuit which can shorten the drawing-in time from an asynchronous state to a synchronous state.

[0016]

[Means for Solving the Problem]A phase synchronous loop circuit concerning this invention outputs the 1st narrow phase difference detecting information of a sweep frequency range after being judged with true phase lock OFF until between existing scheduled time passes, If between the existing scheduled time passes, it is made to output the 2nd phase difference detecting information in which a sweep frequency range is wider than the 1st phase difference detecting information.

[0017]A phase synchronous loop circuit concerning this invention changes a sweep frequency range with reference to phase difference detecting information smoothed by a VCO means.

[0018]

[Embodiment of the Invention]Hereafter, one gestalt of implementation of this invention is explained.

In [embodiment 1. drawing 1 is a lineblock diagram showing the phase synchronous loop circuit by this embodiment of the invention 1, and] a figure, The phase comparator which 11 compares the phase of an input signal and a VCO signal, and outputs the comparison result as phase-difference-detecting-information deltatheta (phase difference detecting means), 12 is a synchronization judging part for phase locks (synchronous judging means) which judges whether the present synchronous state is true phase lock on and whether it is true phase lock OFF based on phase-difference-detecting-information deltatheta outputted from the phase comparator 11.

[0019]The synchronization judging part for sweep range control which supervises transition of a synchronous state in order that 13 may determine the sweep range, The narrow sweep reversal information on the sweep frequency range (the 1st phase difference detecting information) is outputted after 14 is judged to be true phase lock OFF until between existing scheduled time passes, When between the existing scheduled time passes, it is a sweep range control section which outputs the sweep reversal information (the 2nd phase difference detecting information) that the sweep frequency range is wider than the 1st phase difference detecting information. The sweep means comprises the synchronization judging part 13 for sweep range control, and the sweep range control section 14.

[0020]When 15 is judged by the synchronization judging part 12 for phase locks to be the phase lock on of truth [synchronous state], It outputs to the loop filter 16 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 11, The phase contrast control section outputted to the loop filter 16 by making into the phase contrast control information deltathetaout the sweep inversion signal outputted from the sweep range control section 14 when a synchronous state is judged to be true phase lock OFF, The loop filter which smooths the phase contrast control information deltathetaout to which 16 was outputted

from the phase contrast control section 15, and 17 are VCO which outputs as a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 16. The VCO means comprises the phase contrast control section 15, the loop filter 16, and VCO17.

[0021]Next, operation is explained. Operation of the closed-loop processing in a phase synchronous loop circuit is explained to the beginning. First, the phase comparator 11 compares the phase of an input signal and a VCO signal, sets the comparison result to phase-difference-detecting-information deltatheta, and outputs to the synchronization judging part 12 for phase locks, and the phase contrast control section 15.

[0022]The synchronization judging part 12 for phase locks will judge a synchronous state based on the phase-difference-detecting-information deltatheta, if phase-difference-detecting-information deltatheta is received from the phase comparator 11. That is, it is judged whether the present synchronous state is true phase lock on or it is true phase lock OFF. A phase synchronous loop circuit performs closed-loop processing, when the present synchronous state is true phase lock on, when it is true phase lock OFF, perform open loop processing, but. When judged with the decision processing in the synchronization judging part 12 for phase locks having [more than the number of times of regulation] phase-difference-detecting-information deltatheta smaller than the value judged to be phase lock on, it is judged with a true phase lock on state. Conversely, when more than the number of times of regulation judges that phase-difference-detecting-information deltatheta is larger than the value judged to be phase lock OFF, it is judged with a true phase lock OFF state.

[0023]The phase contrast control section 15 will be outputted to the loop filter 16 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 11, if a synchronous state is judged by the synchronization judging part 12 for phase locks to be true phase lock on. This processing is continued until a synchronous state is judged by the synchronization judging part 12 for phase locks to be true phase lock OFF.

[0024]The loop filter 16 will perform data smoothing of the phase contrast control information deltathetaout, if the phase contrast control information deltathetaout is received from the phase contrast control section 15. VCO17 is outputted to the phase comparator 11 by making into a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 16. If repeat execution of each processing in phase comparator 11, phase contrast control-section 15, loop filter 16, and VCO17 is carried out, the phase contrast of an input signal and a VCO signal will decrease gradually, and will become almost the same [the phase of an input signal and a VCO signal], and a phase lock will be materialized.

[0025]Next, operation of the open loop processing in a phase synchronous loop circuit is explained. Since the processing in phase comparator 11, synchronization judging part 12 for phase locks, phase control part 15, loop filter 16, and VCO17 is the same as that of the case of closed-loop processing, explanation is omitted. The synchronization judging part 13

for sweep range control supervises transition of a synchronous state based on the true phase lock ON-and-OFF information and lapsed time of the synchronization judging part 12 for phase locks, in order to determine the sweep range.

[0026]Here, drawing 2 is an explanatory view showing transition of a synchronous state. The transition to the forward alignment guard time B for sweep ranges changes from the synchronous formation A for sweep ranges by detecting phase lock OFF of the truth of the synchronization judging part 12 for phase locks. The transition to the synchronous formation A for sweep ranges changes from the forward alignment guard time B for sweep ranges by detecting the true phase lock on of the synchronization judging part 12 for phase locks.

[0027]The transition to step-out C for sweep ranges from the forward alignment guard time B for sweep ranges changes by not detecting the true phase lock on of the forward-alignment-guard-time prescribed period for sweep ranges, and the synchronization judging part 12 for phase locks. The transition to the method protection D of after use [sweep range] changes from step-out for sweep ranges C by detecting the true phase lock on of the synchronization judging part 12 for phase locks. The transition to step-out C for sweep ranges from the method protection D of after use [sweep range] changes by detecting phase lock OFF of the truth of the synchronization judging part 12 for phase locks.

[0028]The transition to the synchronous formation A for sweep ranges changes from the method protection D of after use [sweep range] by not detecting phase lock OFF of the truth of the method protection prescribed period of after use [sweep range], and the synchronization judging part 12 for phase locks. In the forward alignment guard time B for sweep ranges, make the forward-alignment-guard-time prescribed period for sweep ranges for example, into 72 clock width, and let the method protection prescribed period of after use [sweep range] be for example, 4 clock width in the method protection D of after use [sweep range]. The synchronous determination information for sweep ranges which is a monitored result of these transition is outputted to the sweep range control section 14.

[0029]At this Embodiment 1, the synchronous state for sweep ranges is controlled by the state where it is thought like [immediately after truth carries out phase lock OFF] that frequency has seldom shifted not to sweep all the sweep ranges as a state of the forward alignment guard time B for sweep ranges, but to sweep only in little range. That is, if the synchronous determination information for sweep ranges is received from the synchronization judging part 13 for sweep range control, the sweep range control section 14 will determine the sweep range, as shown below. In the state of step-out C for sweep ranges, it controls so that the sweep range becomes large, and sweep control is not carried out in the state of the method protection D of after use [sweep range], and the synchronous formation A for sweep ranges. In the state of the forward alignment guard time B for sweep ranges, it controls so that the sweep range becomes small.

[0030]Control of the sweep range is performed using a counter. Sweep reversal information is outputted to regulation count number **** et al. and the phase contrast control section 15,

and this is repeated. However, the first time outputs sweep reversal information by one half of regulation count numbers. For example, in the state of the forward alignment guard time B for sweep ranges, it controls so that a sweep direction is reversed at intervals of 24 clocks. In the state of step-out C for sweep ranges, to be able to sweep a total range, it controls so that a sweep direction is reversed at intervals of 10000 clocks.

[0031]Drawing 3 shows the example of level luffing motion by Embodiment 1 and conventional technology. After truth carries out the phase lock on of the example of level luffing motion of drawing 3, it is judged by noise etc. to be true phase lock OFF, and serves as sweep processing of an open loop, In the position which crosses the input frequency of a phase synchronous loop circuit, it draws in the 1st time, it goes wrong, it draws in the position which crosses the 2nd time with the input frequency of a phase synchronous loop circuit, and a success is shown. In this example, since the frequency sweep is performed in the range whose level-luffing-motion frequency X in Embodiment 1 is narrower than the level-luffing-motion frequency Y in conventional technology, it turns out that it settled in the frequency of the input signal of a phase synchronous loop circuit quickly, and has retracted more quickly than conventional technology.

[0032]Above, the 1st narrow phase difference detecting information of the sweep frequency range is outputted according to this Embodiment 1, after being judged with true phase lock OFF until between existing scheduled time passes, so that clearly, Since it constituted so that the 2nd phase difference detecting information in which the sweep frequency range is wider than the 1st phase difference detecting information might be outputted when between the existing scheduled time passed, the effect that the drawing-in time from an asynchronous state to a synchronous state can be shortened is done so.

[0033]Although the embodiment 2. above-mentioned embodiment 1 showed what determines the sweep frequency range in consideration of the lapsed time after being judged with true phase lock OFF, It may be made for the sweep range control section 18 (sweep means) to change the sweep frequency range with reference to the phase difference detecting information (loop filter output voltage) smoothed with the loop filter 16, as shown in drawing 4.

[0034]That is, in the sweep range control section 18, the loop filter output voltage from the synchronous determination information for sweep ranges and the loop filter 16 from the synchronization judging part 13 for sweep range control determines the sweep range. The sweep range control section 18 memorizes the output voltage of the loop filter 16 in the state of the synchronous formation A for sweep ranges, and, specifically, sweeps focusing on the output voltage of the memorized loop filter 16 at the time of the forward alignment guard time B for sweep ranges. For example, in the state of the forward alignment guard time B for sweep ranges, it controls to sweep the range of **0.3V of the output voltage in the state of the synchronous formation A for phase locks, and to sweep a total range in the state of step-out C for sweep ranges.

[0035]The state where it is thought like [in this Embodiment 2 / immediately after truth

carries out phase lock OFF] that frequency has seldom shifted, It controls to sweep only in little range centering on the frequency which did not sweep all the sweep ranges as a state of the forward alignment guard time B for sweep ranges, but locked the synchronous state for sweep ranges before. In this case, since the output voltage of the loop filter 16 is observed, the more exact frequency sweep range is controllable.

[0036]Drawing 5 shows the example of level luffing motion by Embodiment 2 and conventional technology. After truth carries out the phase lock on of the example of level luffing motion of drawing 5, it is judged by noise etc. to be true phase lock OFF, and serves as sweep processing of an open loop, In the position which crosses the input frequency of a phase synchronous loop circuit, it draws in the 1st time, it goes wrong, it draws in the position which crosses the 2nd time with the input frequency of a phase synchronous loop circuit, and a success is shown.

[0037]In this example, a frequency sweep is performed in the range whose level-luffing-motion frequency Z in Embodiment 2 is narrower than the level-luffing-motion frequency Y in conventional technology, And since it has swept focusing on the input frequency of the phase synchronous loop circuit memorized at synchronous formation A:00 for sweep ranges, it turns out that it settled in the frequency of the input signal of a phase synchronous loop circuit quickly, and has retracted more quickly than conventional technology.

[0038]Therefore, since this Embodiment 2 sweeps more correctly than the above-mentioned Embodiment 1 the sweep range suitable for the synchronous state for sweep ranges, it can make still quicker level-luffing-motion time of a phase synchronous loop circuit.

[0039]

[Effect of the Invention]As mentioned above, according to this invention, the 1st narrow phase difference detecting information of the sweep frequency range is outputted after being judged with true phase lock OFF until between existing scheduled time passes, Since it constituted so that the 2nd phase difference detecting information in which the sweep frequency range is wider than the 1st phase difference detecting information might be outputted when between the existing scheduled time passed, it is effective in the ability to shorten the drawing-in time from an asynchronous state to a synchronous state.

[0040]According to this invention, since it constituted so that the sweep frequency range might be changed with reference to the phase difference detecting information smoothed by the VCO means, it is effective in the ability to shorten further the drawing-in time from an asynchronous state to a synchronous state.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention]When this invention will be in an asynchronous state, it relates to the phase synchronous loop circuit drawn in a synchronous state using the phase difference detecting information for a sweep.

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PRIOR ART

[Description of the Prior Art]A phase synchronous loop circuit is also called PLL (Phase Locked Loop), and performs closed-loop processing which comprises a phase comparator, a loop filter, and VCO. Generally, in a phase-locked loop, when the frequency of an input signal and a VCO signal differs extremely, special processing called the sweep processing using open loop processing may be performed.
[0003]In [drawing 6 is a lineblock diagram showing the conventional phase synchronous loop circuit shown in JP,2-100348,A, and] a figure, The phase comparator which 1 compares the phase of an input signal and a VCO signal, and outputs the comparison result as phase-difference-detecting-information deltatheta, The synchronization judging part for phase locks which judges a synchronous state based on phase-difference-detecting-information deltatheta to which 2 was outputted from the phase comparator 1, 3 is a sweep range control section which outputs sweep reversal information (phase contrast control information for a sweep), when a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.
[0004]When 4 is judged by the synchronization judging part 2 for phase locks to be the phase lock on of truth [synchronous state], It outputs to the loop filter 5 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 1, The phase contrast control section outputted to the loop filter 5 by making into the phase contrast control information deltathetaout the sweep inversion signal outputted from the sweep range control section 3 when a synchronous state is judged to be true phase lock OFF, The loop filter which smooths the phase contrast control information deltathetaout to which 5 was outputted from the phase contrast control section 4, and 6 are VCO which outputs as a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 5.
[0005]Next, operation is explained. Operation of the closed-loop processing in a phase synchronous loop circuit is explained to the beginning. First, the phase comparator 1 compares the phase of an input signal and a VCO signal, sets the comparison result to

phase-difference-detecting-information deltatheta, and outputs to the synchronization judging part 2 for phase locks, and the phase contrast control section 4.

[0006]The synchronization judging part 2 for phase locks will judge a synchronous state based on the phase-difference-detecting-information deltatheta, if phase-difference-detecting-information deltatheta is received from the phase comparator 1. That is, it is judged whether the present synchronous state is true phase lock on or it is true phase lock OFF. A phase synchronous loop circuit performs closed-loop processing, when the present synchronous state is true phase lock on, when it is true phase lock OFF, perform open loop processing, but. When judged with the decision processing in the synchronization judging part 2 for phase locks having [more than the number of times of regulation] phase-difference-detecting-information deltatheta smaller than the value judged to be phase lock on, it is judged with a true phase lock on state. Conversely, when more than the number of times of regulation judges that phase-difference-detecting-information deltatheta is larger than the value judged to be phase lock OFF, it is judged with a true phase lock OFF state.

[0007]The phase contrast control section 4 will be outputted to the loop filter 5 by making into the phase contrast control information deltathetaout phase-difference-detecting-information deltatheta outputted from the phase comparator 1, if a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock on. This processing is continued until a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.

[0008]The loop filter 5 will perform data smoothing of the phase contrast control information deltathetaout, if the phase contrast control information deltathetaout is received from the phase contrast control section 4. VCO6 is outputted to the phase comparator 1 by making into a subcarrier the VCO signal which has the phase difference information of the minus smoothed with the loop filter 5. If repeat execution of each processing in phase comparator 1, phase contrast control-section 4, loop filter 5, and VCO6 is carried out, the phase contrast of an input signal and a VCO signal will decrease gradually, and will become almost the same [the phase of an input signal and a VCO signal], and a phase lock will be materialized.

[0009]Next, operation of the open loop processing in a phase synchronous loop circuit is explained. Since the processing in phase comparator 1, synchronization judging part 2 for phase locks, loop filter 5, and VCO6 is the same as that of the case of closed-loop processing, explanation is omitted. The sweep range control section 3 will output sweep reversal information (phase contrast control information for a sweep) to the phase contrast control section 4, if a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF.

[0010]The sweep range control section 3 outputs sweep reversal information to the phase contrast control section 4 so that the phase contrast of the output signal of the loop filter 5 may repeat with increase [in increase -> reduction ->] ->--. This processing is mainly performed using a counter, the time of the decision result of the synchronization judging

part 2 for phase locks becoming true phase lock OFF is made into a trigger, and whenever it counts only regulation counted value, the polarity of sweep reversal information is reversed.

[0011]If a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock OFF, the phase contrast control section 4, It outputs to the loop filter 5 by making into the phase contrast control information deltathetaout the sweep reversal information outputted from the sweep range control section 3, without outputting phase-difference-detecting-information deltatheta outputted from the phase comparator 1. This processing is continued until a synchronous state is judged by the synchronization judging part 2 for phase locks to be true phase lock on.

[0012]Although operation of the loop filter 5 is the same as that of the time of closed-loop processing, the smoothed phase contrast which is an output signal of the loop filter 5 increases [fixed-] or decreases [fixed-] it under the influence of the integrator in the loop filter 5 by the ability to give fixed phase contrast. Since phase contrast is considered to be the differentiation of a phase value, i.e., frequency, that phase contrast increases means that frequency increases. That phase contrast decreases similarly means that frequency decreases.

[0013]Therefore, the frequency of the VCO signal outputted from VCO6 becomes possible [creating the state where it becomes the operation which continues sweeping the normal frequency range, and the frequency and the phase of the input signal and VCO signal of a phase synchronous loop circuit become the same] by inputting fixed phase contrast into the loop filter 5. The frequency of a VCO signal needs to sweep the regulation sweep range of this frequency in the range which can respond even when the frequency of the input signal of a phase synchronous loop circuit shifts.

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EFFECT OF THE INVENTION

[Effect of the Invention]As mentioned above, when the 1st narrow phase difference detecting information of the sweep frequency range was outputted and between the existing scheduled time passed after being judged with true phase lock OFF until between existing scheduled time passed, it constituted from this invention so that the 2nd phase difference detecting information in which the sweep frequency range is wider than the 1st phase difference detecting information might be outputted.
Therefore, it is effective in the ability to shorten the drawing-in time from an asynchronous state to a synchronous state.

[0040]It constituted from this invention so that the sweep frequency range might be changed with reference to the phase difference detecting information smoothed by the VCO means.
Therefore, it is effective in the ability to shorten further the drawing-in time from an asynchronous state to a synchronous state.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]Since the conventional phase synchronous loop circuit is constituted as mentioned above, after the phase lock on of once truth is materialized, when judged with true phase lock OFF by the influence of noise etc., change into an open loop state from closed-loop processing, and perform the frequency sweep of VCO6, but. In order to carry out sweep control of a total range and to sweep to excessive frequency in spite of not shifting frequency greatly when true phase lock OFF has just arisen, the long time was taken to lock true frequency and SUBJECT that level luffing motion took time occurred.
[0015]It was made in order that this invention might solve above SUBJECT, and it aims at obtaining the phase synchronous loop circuit which can shorten the drawing-in time from an asynchronous state to a synchronous state.

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CLAIMS

[Claim(s)]
[Claim 1]A phase difference detecting means which detects phase contrast of an input signal and a VCO signal.
A synchronous judging means which judges a synchronous state based on phase contrast detected by the above-mentioned phase difference detecting means.
A sweep means which outputs phase difference detecting information for a sweep when a synchronous state is judged by the above-mentioned synchronous judging means to be true phase lock OFF.
A VCO means to output a VCO signal according to phase difference detecting information outputted from the above-mentioned sweep means.
Are the above the phase synchronous loop circuit which it had, and the above-mentioned sweep means, If the 1st narrow phase difference detecting information of a sweep frequency range is outputted and between the existing scheduled time passes after being judged with true phase lock OFF until between existing scheduled time passes, the 2nd phase difference detecting information in which a sweep frequency range is wider than the 1st phase difference detecting information will be outputted.

[Claim 2]The phase synchronous loop circuit according to claim 1, wherein a sweep means changes a sweep frequency range with reference to phase difference detecting information smoothed by a VCO means.

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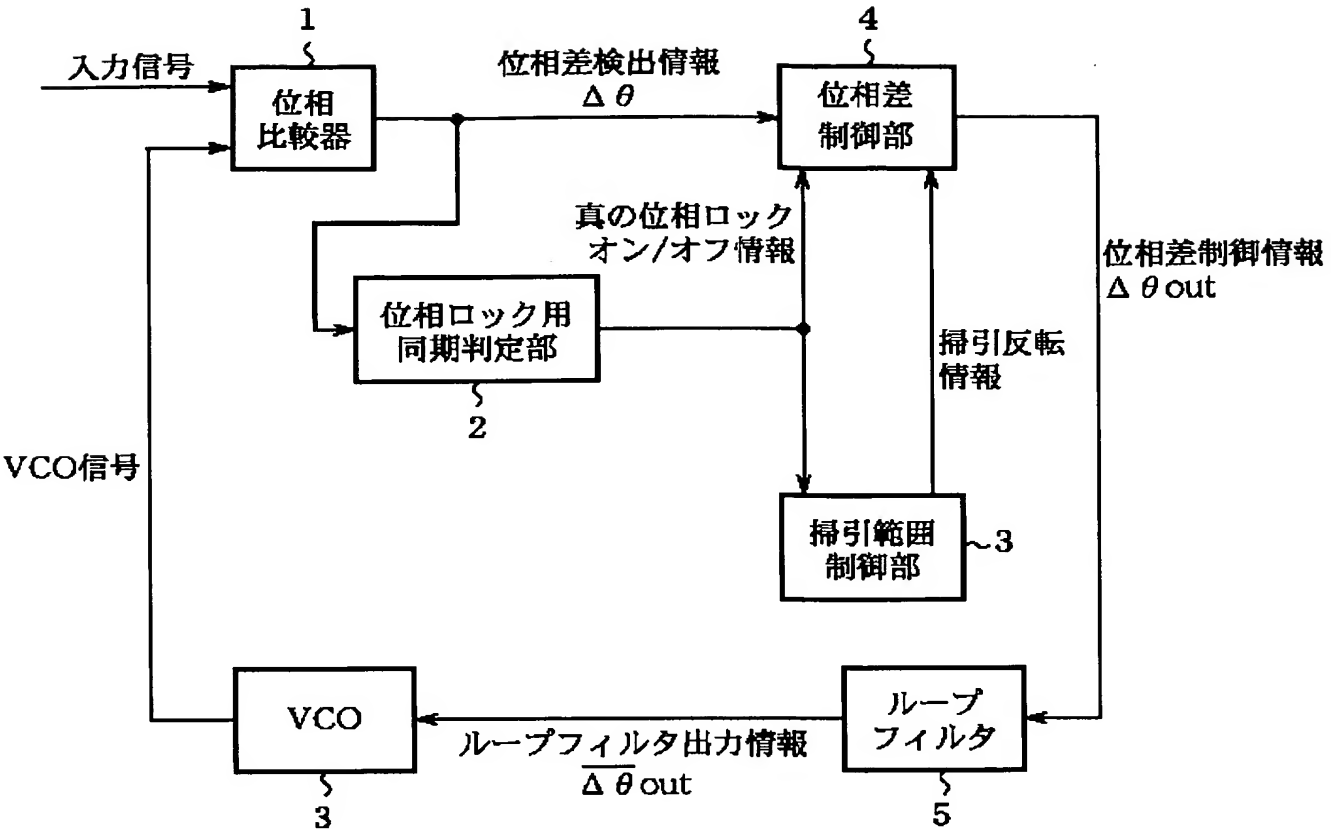
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a lineblock diagram showing the phase synchronous loop circuit by this embodiment of the invention 1.
[Drawing 2]It is an explanatory view showing transition of a synchronous state.
[Drawing 3]It is an explanatory view showing the example of level luffing motion by Embodiment 1 and conventional technology.
[Drawing 4]It is a lineblock diagram showing the phase synchronous loop circuit by this embodiment of the invention 2.
[Drawing 5]It is an explanatory view showing the example of level luffing motion by Embodiment 2 and conventional technology.
[Drawing 6]It is a lineblock diagram showing the conventional phase synchronous loop circuit.
[Description of Notations]
11 A phase comparator (phase difference detecting means), the synchronization judging part for 12 phase locks (synchronous judging means), 13 The synchronization judging part for sweep range control (sweep means), and 14 A sweep range control section (sweep means), 15 phase-contrast control section (VCO means), and 16 A loop filter (VCO means), 17 VCO (VCO means), and 18 Sweep range control section (sweep means).

[Translation done.]


1
入力信号
位相
比較器
位相差検出情報
Δθ
4
位相差
制御部
真の位相ロック
オン/オフ情報
位相差制御情報
Δθout
位相ロック用
同期判定部
2
掃引反転
情報
VCO信号
掃引範囲
制御部
3
VCO
3
ループフィルタ出力情報
Δθout
ループ
フィルタ
5